

What is Claimed is:

1. A display device comprising:

a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

horizontal video start position detection means for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value;

horizontal video end position detection means for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a second threshold value;

calculation means for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position;

judgment means for judging whether or not the result of the calculation by the calculation means

coincides with a required reference value;

frequency control value adjustment means for calculating, when it is judged that the result of the calculation by the calculation means and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation means, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit; and

threshold value control means for controlling a second threshold value depending on the level of the video data outputted from the analog-to-digital converter.

2. The display device according to claim 1, wherein the clock generation circuit comprises

a voltage controlled oscillator for outputting the sampling clocks,

a frequency divider for dividing the frequency of the sampling clocks outputted from the voltage controlled oscillator,

phase detection means, to which an output of the frequency divider and the horizontal synchronizing signal of the input video signal are inputted, for

outputting a detection signal corresponding to the phase difference between both the inputted signals, and

filter means for integrating the detection signal outputted from the phase detection means, to output the integrated detection signal to the voltage controlled oscillator,

the frequency division ratio of the frequency divider being used as the frequency control value.

3. A display device comprising:

a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

a horizontal video start position detection circuit for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value;

a horizontal video end position detection circuit for detecting a horizontal video end

position of the video data outputted from the analog-to-digital converter on the basis of a second threshold value;

a calculation circuit for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position;

a judgment circuit for judging whether or not the result of the calculation by the calculation means coincides with a required reference value;

a frequency control value adjustment circuit for calculating, when it is judged that the result of the calculation by the calculation circuit and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation circuit, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit; and

a threshold value control circuit for controlling a second threshold value depending on the level of the video data outputted from the analog-to-digital converter.

4. The display device according to claim 3,

wherein the clock generation circuit comprises
a voltage controlled oscillator for outputting
the sampling clocks,

a frequency divider for dividing the frequency
of the sampling clocks outputted from the voltage
controlled oscillator,

a phase detection circuit, to which an output
of the frequency divider and the horizontal
synchronizing signal of the input video signal are
inputted, for outputting a detection signal
corresponding to the phase difference between both
the inputted signals, and

a filter circuit for integrating the detection
signal outputted from the phase detection circuit,
to output the integrated detection signal to the
voltage controlled oscillator,

the frequency division ratio of the frequency
divider being used as a frequency control value.

5. A pixel corresponding display device
comprising:

a clock generation circuit for generating
sampling clocks on the basis of a horizontal
synchronizing signal of an input video signal;
an analog-to-digital converter for sampling
the input video signal on the basis of the sampling

clocks generated from the clock generation circuit;

detection means for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

calculation means for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video start positions detected within one field and a horizontal video end position farthest from the horizontal period start position specified by the horizontal synchronizing signal out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

frequency adjustment means for controlling the clock generation circuit on the basis of the result of the calculation by the calculation means, to adjust the frequency of the sampling clocks;

judgment means for judging for each field whether or not the width of a region where input video

exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means; and

means for stopping, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

6. A pixel corresponding display device comprising:

a clock generation circuit for generating sampling clocks on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

a detection circuit for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

a calculation circuit for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of

horizontal video start positions detected within one field and a horizontal video end position farthest from a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

a frequency adjustment circuit for controlling the clock generation circuit on the basis of the result of the calculation by the calculation circuit, to adjust the frequency of the sampling clocks;

a judgment circuit for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation circuit; and

a circuit for stopping, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

7. A pixel corresponding display device

comprising:

a delay circuit, whose amount of delay is variable, for delaying and outputting a horizontal synchronizing signal of an input video signal;

a clock generation circuit for generating sampling clocks which are synchronized with the horizontal synchronizing signal outputted from the delay circuit;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

detection means for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

calculation means for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal outputted from the delay circuit out of horizontal video start positions detected within one field and a horizontal video end position farthest from a horizontal period start position specified by the horizontal synchronizing signal outputted from the delay

circuit out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

phase adjustment means for changing an amount of delay set in the delay circuit a predetermined amount at a time for each field, to change the phase of the sampling clocks a predetermined amount at a time for the field, holding as a first amount of delay the amount of delay set in the delay circuit in the field in a case where the number of sampling clocks calculated by the calculation means is changed in such a direction as to be decreased and holding as a second amount of delay the amount of delay set in the delay circuit in the field in a case where the number of sampling clocks calculated by the calculation means is changed in such a direction as to be increased, and calculating the average sum of the first amount of delay and the second amount of delay, to set the amount of delay set in the delay circuit to the obtained average sum;

judgment means for judging for each field whether or not the width of a region where input video

exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means; and

means for stopping, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels, a phase adjustment operation based on the number of sampling clocks found in the field.

8. A pixel corresponding display device comprising:

a delay circuit, whose amount of delay is variable, for delaying and outputting a horizontal synchronizing signal of an input video signal;

a clock generation circuit for generating sampling clocks which are synchronized with the horizontal synchronizing signal outputted from the delay circuit;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

a detection circuit for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

a calculation circuit for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal outputted from the delay circuit out of horizontal video start positions detected within one field and a horizontal video end position farthest from a horizontal period start position specified by the horizontal synchronizing signal outputted from the delay circuit out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

a phase adjustment circuit for changing an amount of delay set in the delay circuit a predetermined amount at a time for each field, to change the phase of the sampling clocks a predetermined amount at a time for the field, holding as a first amount of delay the amount of delay set in the delay circuit in the field in a case where the number of sampling clocks calculated by the calculation means is changed in such a direction as to be decreased and holding as a second amount of

delay the amount of delay set in the delay circuit in the field in a case where the number of sampling clocks calculated by the calculation circuit is changed in such a direction as to be increased, and calculating the average sum of the first amount of delay and the second amount of delay, to set the amount of delay set in the delay circuit to the obtained average sum;

a judgment circuit for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means; and

a circuit for stopping, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels, a phase adjustment operation based on the number of sampling clocks found in the field.